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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/589,915	CHONG ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14-17 and 19-34* is/are pending in the application.

4a) Of the above claim(s) *22-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14-17,19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendments to the Abstract and Title filed on September 22, 2008 are acknowledged. The objections made the specification in the previous office action filed on May 22, 2008 are withdrawn.

Claim Objections

2. The amendment to claim 8 filed on September 22, 2008 is acknowledged. The objection made to claim 8 in the previous office action filed on May 22, 2008 is withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 - 9, 11, 14 – 17, and 19 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kostylev et al. (US 2004/0026730 A1, prior art of record) in view of Chen (US 2005/0051901 A1, prior art of record), with evidentiary support provided by Hirota et al. (US 5,063,097, prior art of record) and Miyamoto et al. (US 2004/0106065, prior art of record).

a. Regarding claim 1, **Kostylev discloses a data recording element for a memory cell of a writeable and erasable memory medium** (figure 7) **comprising:**

a laminated structure (laminated structure comprising layers 140a - 140d and 150a – 150d) **of at least two multiple-layer structures** (first multiple layer structure 140a and 150a, second multiple layer structure 140b and 150b, and third multiple layer structure 140c and 150c),

each said multiple-layer structure comprising a plurality of individual layers (each multiple layer structure has at least 2 layers, as disclosed above),

at least one of the plurality of individual layers in each multiple layer structure being made of a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse (each layer 140a - 140d is a programmable resistance material, which is particularly a phase changing material between amorphous and crystalline states due to an electrical signal, as disclosed in paragraphs [0003], [0023], [0038], and [0049]), **and**

one of the plurality of individual layers of one of said at least two multiple-layer structures having at least one atomic element which is absent from a second one of said plurality of individual layers (layers 150a – 150e comprise metals such as Ti, V, Nb, Ta, as disclosed in paragraphs [0038] and [0043], while layers 140a – 140d comprise materials such as Te, Ge, and Sb9, as disclosed in paragraphs [0038] and [0050]), **and**

a final individual layer (final individual layer 140d), **disposed upon at least two multiple-layer structures** (e.g. as seen in figure 7, layer 140d is disposed upon the two multiple layer structures comprising layers 150a, 140a, and 150b, 140b), **said final individual layer being formed of the same material as a first of said plurality of individual layers in a first of said at least two multiple-layer structure of said laminated structure** (layer 140d may be of the same material as layer 140a, as disclosed in paragraph [0041]).

Kostylev is silent with respect to wherein a crystallization speed of said first of said plurality of individual layers of said first of said at least two multiple-layer structures and said final individual layer is higher than that of the other ones of said plurality of individual layers of said multiple-layer structure, and a crystallization temperature of said first of said plurality of individual layers of said first of said at least two multiple-layer structures and said final individual layer is lower than other ones of said plurality of individual layers of said first of said at least two multiple-layer structures. Kostylev does disclose materials which may comprise the phase change memory medium (¶ [0050] - [0052] for the phase change material in layers 140a,b,c,d (¶ [0038]) and paragraphs [0042] - [0047] for the material of stabilizing layers 150a,b,c,d (¶ [0038])).

Chen discloses a data recording element (as seen in figure 3, with reference to figures 4a - 4g and 5) **wherein a crystallization speed of said first individual layer** (layer 22d) **and final individual layer** (layer 22a) **is higher**

than that of other layers (lattice mismatch layers 24) **of the multiple-layer structure** (¶ [0030] discloses layers 22d and 22a to be made of $Ge_2Sb_2Te_5$ and layers 24 to be made of GeTe. ¶ [0032] discloses that the crystallization process through layers 24 lag the crystallization process through phase change material layers 22 (a – d). Therefore, the crystallization speed through the phase change layers 22a and 22d is higher than the mismatch layers 24)**, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure** (Hirota discloses the crystallization temperature of $Ge_2Sb_2Te_5$ to be 142^oC (col. 11, lines 66 - 68), and Miyamoto discloses the crystallization temperature of GeTe to be 200^oC (¶ [0071]). Therefore, the crystallization temperature of the first and final individual layers 22d and 22a, made of $Ge_2Sb_2Te_5$, is lower than the crystallization temperatures of the other layers 24, made of GeTe)**.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev such that the first and final individual layers have a higher crystallization speed and lower crystallization temperature since it was shown by Chen that such devices using phase change material for data recording were known in the art. One would have been motivated to make such a device since a phase change material with a lower crystallization temperature and higher crystallization speed on the first and final layers would yield a device with a fast response with lower power consumption, while maintaining structural integrity (as disclosed in paragraph [0055] of

Kostylev), as well as preventing the phase change materials from merging with the lattice mismatch materials (as disclosed in ¶ [0030] of Chen).

b. Regarding claim 2, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, wherein the plurality of individual layers in a first one and a second one of said at least two multiple-layer structures are disposed in a same sequence** (Kostylev: as seen in figure 7).

c. Regarding claim 3, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, wherein the plurality of individual layers in a first one and a second one of said at least two multiple-layer structures are disposed in a different sequence** (Kostylev: ¶ [0041] discloses variations of the memory stack layering of figure 7).

d. Regarding claim 4, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, but are silent with respect to explicitly stating that each of said plurality of layers in each of said at least two multiple-layer structures has a thickness in a range of about 0.1 nm to about 10 nm**. **However, ¶ [0048] of Kostylev discloses the stabilization layers 150a – 150e to be <u>less than</u> 5nm thick, and ¶ [0053]**

discloses the programmable resistance material layers 140a – 140d to be less than 17.5 nm thick.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev in view Chen such that the layers were smaller in thickness than explicitly disclosed by Kostylev, since Kostylev teaches that the layers may be smaller than a thickness close to the claimed thickness, and it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05. One would have been motivated to decrease the layer thickness of Kostylev in order to reduce device size and use less material to reduce manufacturing costs.

e. Regarding claim 5, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, but are silent with respect to each of the individual layers in each of said at least two multiple-layer structures have the same thickness. However, ¶ [0048] of Kostylev discloses the stabilization layers 150a – 150e to be less than 5nm thick, and paragraph [0053] discloses the programmable resistance material layers 140a – 140d to be less than 17.5 nm thick.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev in view Chen such that the layers were equal in thickness, since Kostylev teaches that the layers may be

within the same range (i.e.. less than 17.5 nm thick), and it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05. One would have been motivated to create equal layer thicknesses of Kostylev in order to create a consistent device and minimize differences in manufacturing steps.

f. Regarding claim 6, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, wherein any two adjacent ones of the plurality of individual layers in one of said at least two multiple-layer structures have a ratio of thickness in a range of about 0.1 to about 10** (Kostylev: ¶ [0048] and [0053]).

g. Regarding claim 7, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, wherein the total thickness of the data recording element is in a range of about 5 nm to about 500 nm** (Kostylev: ¶ [0054] discloses the total thickness is less than 80 nm).

h. Regarding claim 8, **Kostylev discloses the data recording element as recited in claim 1, as cited above, wherein the total thickness of the data**

recording element is in a range of about 5 nm to 100 nm (Kostylev: ¶ [0054] discloses the total thickness is less than 80 nm).

i. Regarding claim 9, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, wherein at least one of the plurality of individual layers is formed of a material selected from a group consisting of Ge, Te, Sb, GeTe, SbTe, AgIn, GcSbTe, AgInSbTe, TeAsGe, TeSeS, TeSeSb, InSbTe, TeGeSn, In, Cr, N, Se, Sn, Si, Bi and Ag** (¶ [0050] of Kostylev discloses the programmable resistance layers to comprise Te, Ge, Sb, and other materials).

j. Regarding claim 11, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, wherein a resistance of said at least one of said plurality of individual layers is lower in a crystalline state-than that in an amorphous state** (Kostylev incorporates U.S. Patent 5,166,758 by reference in paragraph [0049]. Patent 5,166,758 discloses the layers of a phase changing material to have a lower resistance in the crystalline state than in the amorphous state in col. 4, lines 35 - 43).

k. Regarding claim 14, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, but are silent with respect to explicitly stating the crystallization temperature of said first of**

first of said plurality of individual layers in said first of said at least two multiple-layer structures of said laminated structure is in a range of about 90°C to 120°C. However, Kostylev discloses the material used in the memory layers to comprise Ge, Sb, Bi, Pb, Sn, and other known phase change materials (¶ [0050]). **Chen also discloses the materials of memory layers to be $Ge_2Sb_2Te_5$** (¶ [0030]). **Hirota discloses the crystallization temperature of $Ge_2Sb_2Te_5$ to be 142°C** (col. 11, lines 66 – 68).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the materials of the first of the plurality of individual layers of the multiple layer structures such that the crystallization temperature was within a range of 90°C to 120°C since Chen teaches layers may comprise materials with a crystallization temperature close to that range, and it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05. One would have been motivated to have a crystallization temperature within the claimed range in order to have a device that can operate with less power consumption, as well as dissipating less heat.

l. Regarding claim 15, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, further comprising an electrode formed adjacent to the data recording element** (Kostylev:

electrode 110, disclosed in ¶ [0029]), **an edge of the electrode contacting the data recording element for transferring electrical signals between the electrode and the data recording element** (Kostylev: e.g. as seen in figure 7).

m. Regarding claim 16, **Kostylev in view of Chen disclose the data recording element as recited in claim 1, wherein said laminated structure forms a superlattice-like structure** (e.g. as seen in figure 7 of Kostylev, the structure has alternating layers of phase changing material, and thus is a superlattice, as defined on pages 9 and 10 of the current application's specification).

n. Regarding claim 17, **Kostylev discloses a data recording element for a memory cell of a writeable and erasable memory medium** (e.g. figure 7) **comprising:**

a laminated structure (laminated structure comprising layers 140a - 140d and 150a – 150d) **having a first external layer** (layer 140a), **a second external layer** (external layer 140d) **and a plurality of internal layers** (internal layers 150b, 150c, and 150d) formed between the first and second external layers (as seen in the figure), **at least one layer of the laminated structure being made of a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse** (each layer 140a - 140d is a programmable resistance material, which is particularly a phase changing

material between amorphous and crystalline states due to an electrical signal, as disclosed in paragraphs [0003], [0023], [0038], and [0049]).

Kostylev is silent with respect to explicitly disclosing said first and second external layers have a relatively higher crystallization speed and lower crystallization temperature than the plurality of internal layers.

Chen discloses a data recording element (as seen in figure 3, with reference to figures 4a - 4g and 5) **wherein a crystallization speed of said first individual layer** (layer 22d) **and final individual layer** (layer 22a) **is higher than that of other layers** (lattice mismatch layers 24) **of the multiple-layer structure** (¶ [0030] discloses layers 22d and 22a to be made of $Ge_2Sb_2Te_5$ and layers 24 to be made of GeTe. ¶ [0032] discloses that the crystallization process through layers 24 lag the crystallization process through phase change material layers 22 (a – d). Therefore, the crystallization speed through the phase change layers 22a and 22d is higher than the mismatch layers 24)**, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure** (Hirota discloses the crystallization temperature of $Ge_2Sb_2Te_5$ to be 142^{o}C (col. 11, lines 66 - 68), and Miyamoto discloses the crystallization temperature of GeTe to be 200^{o}C (¶ [0071]). Therefore, the crystallization temperature of the first and final individual layers 22d and 22a, made of $Ge_2Sb_2Te_5$, is lower than the crystallization temperatures of the other layers 24, made of GeTe).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev such that the first and final individual layers have a higher crystallization speed and lower crystallization temperature since it was shown by Chen that such devices using phase change material for data recording were known in the art. One would have been motivated to make such a device since a phase change material with a lower crystallization temperature and higher crystallization speed on the first and final layers would yield a device with a fast response with lower power consumption, while maintaining structural integrity (as disclosed in paragraph [0055] of Kostylev), as well as preventing the phase change materials from merging with the lattice mismatch materials (as disclosed in ¶ [0030] of Chen).

o. Regarding claim 19, **Kostylev in view of Chen disclose the data recording element as recited in claim 17, as cited above, but are silent with respect to explicitly stating the crystallization temperature of said first and second external layers is in a range of about 90°C to 120°C. However, Kostylev discloses the material used in the memory layers to comprise Ge, Sb, Bi, Pb, Sn, and other known phase change materials** (¶ [0050]). **Chen also discloses the materials of memory layers to be $Ge_2Sb_2Te_5$** (¶ [0030]). **Hirota discloses the crystallization temperature of $Ge_2Sb_2Te_5$ to be 142°C** (col. 11, lines 66 – 68).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the materials of the first of the plurality of individual layers of the multiple layer structures such that the crystallization temperature was within a range of 90°C to 120°C since Chen teaches layers may comprise materials with a crystallization temperature close to that range, and it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05. One would have been motivated to have a crystallization temperature within the claimed range in order to have a device that can operate with less power consumption, as well as dissipating less heat.

p. Regarding claim 20, **Kostylev discloses a memory cell for a writeable and erasable memory medium** (figure 7) **comprising:**

a substrate (substrate 100);

first and second contacts formed on said substrate (contacts 110 and 160, disclosed in paragraph [0035]);

a data recording element formed between said first and second contacts (data recording element comprising layers 140a – 140d, and 150a – 150e),

said data recording element comprising a laminated structure of two or more multiple-layer structures (first multiple layer structure 140a and 150b,

second multiple layer structure 140b and 150c, and third multiple layer structure 140c and 150d)**, and a final layer disposed upon said at least two multiple-layer structures** (layer 140d),

each of said at least two multiple-layer structures comprising a plurality of sequentially disposed individual layers (each multiple layer structure has at least 2 layers, as seen in figure 7),

at least one of said plurality of sequentially disposed individual layers in each multiple-layer structures being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse (each layer 140a - 140d is a programmable resistance material, which is particularly a phase changing material between amorphous and crystalline states due to an electrical signal, as disclosed in paragraphs [0003], [0023], [0038], and [0049]),

one of the plurality of sequentially disposed individual layer having at least one atomic element which is absent from a second one of the plurality of individual layers (layers 150a – 150e comprise metals such as Ti, V, Nb, Ta, as disclosed in paragraphs [0038] and [0043], while layers 140a – 140d comprise materials such as Te, Ge, and Sb9, as disclosed in paragraphs [0038] and [0050]);

said final individual layer being formed of the same material as a first of said plurality of sequentially disposed individual layers in a first of said

at least two multiple-layer structures of said laminated structure (final layer 140d is the same material as 104a, as disclosed ¶ [0038]),

a high temperature electrode formed adjacent the data recording element (paragraph [0059] discloses the memory cell to have one or more electrodes, and paragraph [0029] discloses the electrodes to be made of tungsten, which is a high temperature material); **and**

an insulating material isolating said memory cell from adjacent memory cells (dielectric material 120).

Kostylev is silent with respect to explicitly disclosing a crystallization speed of said first of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and said final individual layer is higher than that of other ones of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and a crystallization temperature of said first of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and said final individual layer is lower that other ones of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures. Kostylev does disclose materials which may comprise the phase change memory medium (¶ [0050] - [0052] for the phase change material in layers 140a,b,c,d (¶ [0038]) and paragraphs [0042] - [0047] for the material of stabilizing layers 150a,b,c,d (¶ [0038])).

Chen discloses a data recording element (as seen in figure 3, with reference to figures 4a - 4g and 5) **wherein a crystallization speed of said first individual layer** (layer 22d) **and final individual layer** (layer 22a) **is higher than that of other layers** (lattice mismatch layers 24) **of the multiple-layer structure** (¶ [0030] discloses layers 22d and 22a to be made of $Ge_2Sb_2Te_5$ and layers 24 to be made of GeTe. ¶ [0032] discloses that the crystallization process through layers 24 lag the crystallization process through phase change material layers 22 (a – d). Therefore, the crystallization speed through the phase change layers 22a and 22d is higher than the mismatch layers 24)**, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure** (Hirota discloses the crystallization temperature of $Ge_2Sb_2Te_5$ to be 142^oC (col. 11, lines 66 - 68), and Miyamoto discloses the crystallization temperature of GeTe to be 200^oC (¶ [0071]). Therefore, the crystallization temperature of the first and final individual layers 22d and 22a, made of $Ge_2Sb_2Te_5$, is lower than the crystallization temperatures of the other layers 24, made of GeTe)**.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev such that the first and final individual layers have a higher crystallization speed and lower crystallization temperature since it was shown by Chen that such devices using phase change material for data recording were known in the art. One would have been motivated to make such a device since a phase change material with a lower

crystallization temperature and higher crystallization speed on the first and final layers would yield a device with a fast response with lower power consumption, while maintaining structural integrity (as disclosed in paragraph [0055] of Kostylev), as well as preventing the phase change materials from merging with the lattice mismatch materials (as disclosed in ¶ [0030] of Chen).

q. Regarding claim 21, **Kostylev discloses an electrically writeable and erasable memory medium** (figure 2A) **comprising**

a plurality of memory cells (memory cells 20) **and an arrangement of conductors** (conductors 24) **such that each of said plurality of memory cells is electrically addressable** (as disclosed in paragraph [0025]), each said memory cell (figure 7) **comprising:**

a substrate (substrate 100);

first and second contacts formed on said substrate (contacts 110 and 160, disclosed in paragraph [0035]);

a data recording element formed between said first and second contacts (data recording element comprising layers 140a – 140d, and 150a – 150e),

said data recording element comprising a laminated structure of two or more multiple-layer structures (first multiple layer structure 140a and 150b, second multiple layer structure 140b and 150c, and third multiple layer structure 140c and 150d),

and a final individual layer disposed upon said at least two multiple-layer structures (layer 140d);

each of said at least two multiple-layer structures comprising a plurality of sequentially disposed individual layers (each multiple layer structure has at least 2 layers, as seen in figure 7),

at least one of said plurality of sequentially disposed individual layers in each said at least two multiple-layer structures being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse (each layer 140a - 140d is a programmable resistance material, which is particularly a phase changing material between amorphous and crystalline states due to an electrical signal, as disclosed in paragraphs [0003], [0023], [0038], and [0049]);

one of the plurality of sequentially disposed individual layers having at least one atomic element which is absent from a second one of the plurality of sequentially disposed individual layers (layers 150a – 150e comprise metals such as Ti, V, Nb, Ta, as disclosed in paragraphs [0038] and [0043], while layers 140a – 140d comprise materials such as Te, Ge, and Sb9, as disclosed in paragraphs [0038] and [0050]),

said final individual layer being formed of the same material as a first of said plurality of sequentially disposed individual layers in a first of said at least two multiple-layer structures of said laminated structure (final layer 140d is the same material as 104a, as disclosed ¶ [0038]),

a high temperature electrode formed adjacent the data recording element (paragraph [0059] discloses the memory cell to have one or more electrodes, and paragraph [0029] discloses the electrodes to be made of tungsten, which is a high temperature material); **and**

an insulating material isolating said memory cell from adjacent memory cells (dielectric material 120).

Kostylev is silent with respect to explicitly disclosing a crystallization speed of said first of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and said final individual layer is higher than that of other ones of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and a crystallization temperature of said first of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and said final individual layer is lower that other ones of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures. Kostylev does disclose materials which may comprise the phase change memory medium (¶ [0050] - [0052] for the phase change material in layers 140a,b,c,d (¶ [0038]) and paragraphs [0042] - [0047] for the material of stabilizing layers 150a,b,c,d (¶ [0038])).

Chen discloses a data recording element (as seen in figure 3, with reference to figures 4a - 4g and 5) **wherein a crystallization speed of said first**

individual layer (layer 22d) **and final individual layer** (layer 22a) **is higher than that of other layers** (lattice mismatch layers 24) **of the multiple-layer structure** (¶ [0030] discloses layers 22d and 22a to be made of $Ge_2Sb_2Te_5$ and layers 24 to be made of GeTe. ¶ [0032] discloses that the crystallization process through layers 24 lag the crystallization process through phase change material layers 22 (a – d). Therefore, the crystallization speed through the phase change layers 22a and 22d is higher than the mismatch layers 24)**, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure** (Hirota discloses the crystallization temperature of $Ge_2Sb_2Te_5$ to be 142°C (col. 11, lines 66 - 68), and Miyamoto discloses the crystallization temperature of GeTe to be 200°C (¶ [0071]). Therefore, the crystallization temperature of the first and final individual layers 22d and 22a, made of $Ge_2Sb_2Te_5$, is lower than the crystallization temperatures of the other layers 24, made of GeTe)**.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev such that the first and final individual layers have a higher crystallization speed and lower crystallization temperature since it was shown by Chen that such devices using phase change material for data recording were known in the art. One would have been motivated to make such a device since a phase change material with a lower crystallization temperature and higher crystallization speed on the first and final layers would yield a device with a fast response with lower power consumption,

while maintaining structural integrity (as disclosed in paragraph [0055] of Kostylev), as well as preventing the phase change materials from merging with the lattice mismatch materials (as disclosed in ¶ [0030] of Chen).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kostylev in view of Chen as applied to claim 1 above, and further in view of Sandhu et al (US 5,837,564, prior art of record). **Kostylev in view of Chen disclose the data recording element as recited in claim 1, as cited above, but are silent with respect to at least one of the plurality of individual layers is deposited in a crystalline state.**

Sandhu discloses that layers of memory material comprising chalcogenides (Kostylev discloses the memory material of his device to also comprise chalcogenides such as Te in paragraph [0050]) **may be deposited in a crystalline state** (col. 2, lines 18 – 19).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kostylev in view of Chen such that the individual memory layers are deposited in a crystalline state, since it was known that such memory layers can be formed in such manner, as disclosed by Sandhu. One would have been motivated to make the layers in a crystalline state since it would yield a more consistent and predictable device (Sandhu: col. 2, lines 31 - 35).

Response to Arguments

6. Applicant's arguments filed on September 22, 2008 have been fully considered but they are not persuasive. At present, the prior art of Kostylev in view of Chen remains commensurate to the scope of the claims as stated by the Applicant within the context of the claim language and as broadly interpreted by the Examiner [MPEP 2111], which is elucidated and expounded upon above. In response to Applicants arguments drawn to the amendment, "*A final individual layer disposed upon at least two multiple-layer structures, said final individual layer being formed of the same material as a first of said plurality of individual layers in a first of said at least two multiple-layer structures of said laminated structure wherein a crystallization speed of said first of said plurality of individual layers of said first of said at least two multiple-layer structures and said final individual layer is higher than that of other ones of said plurality of individual layers of said first multiple layer structure and a crystallization temperature of said first of said plurality of individual layers of said first of said at least two multiple-layer structures and said final individual layer is lower that other ones of said plurality of individual layers of said first of said at least two multiple-layer structures*", this added claim limitation is a combined limitation of claims 12 and 13, which where were previously rejected. The Applicant has argued that Kostylev does not teach that the end layers are resistance materials, and that they are not of the same material. However, figure 7 of Kostylev clearly shows end layers 140a and 140d, which are disclosed in ¶ [0038] to be of the same resistance material. Claim 13 was rejected in the prior office action as an obvious limitation of the structure of Kostylev in view of the teachings of Chen. Although the

Applicant states that Kostylev does not disclose such limitations, the Applicant has not presented an argument regarding the rejection of claim 13 of Kostylev *in view of Chen*, as cited in the prior office action. Claim 1 stands rejected over Kostylev in view of Chen.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
December 8, 2008